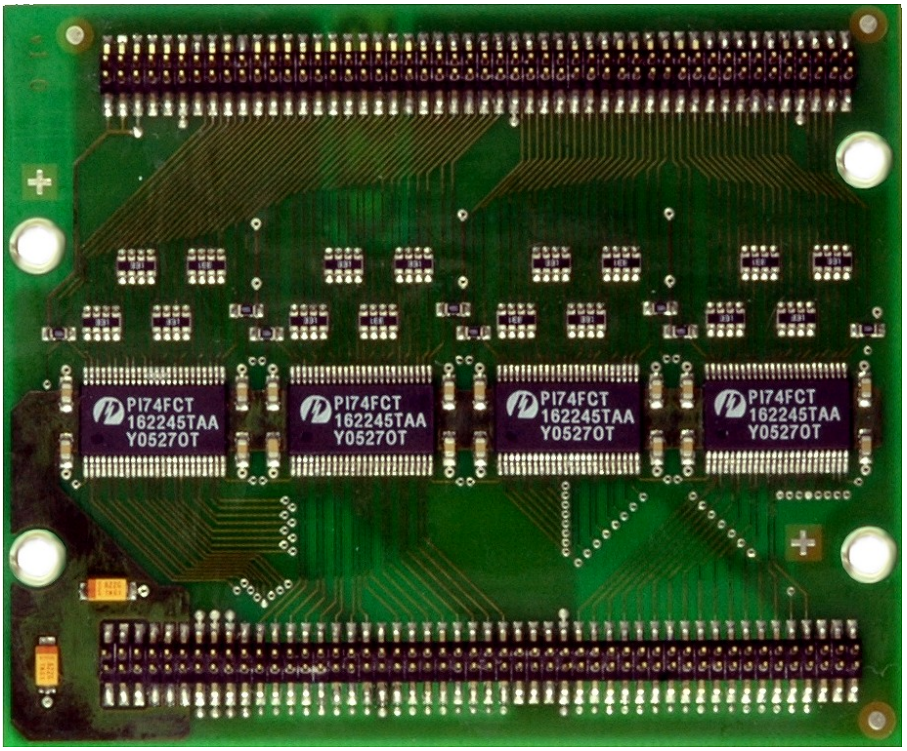
Plugable Interface board with 64 digital channels

Order number: C1050-3506



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Overview

The PIB64IO functions as daughterboard to the CESYS Base Series cards (i.e. PCIS3BASE and PCIeV4BASE). It provides 64 TTL compatible IOs, organized in 8 banks. Each bank can be switched between Input and Output mode. Each bank has its own output enable signal.

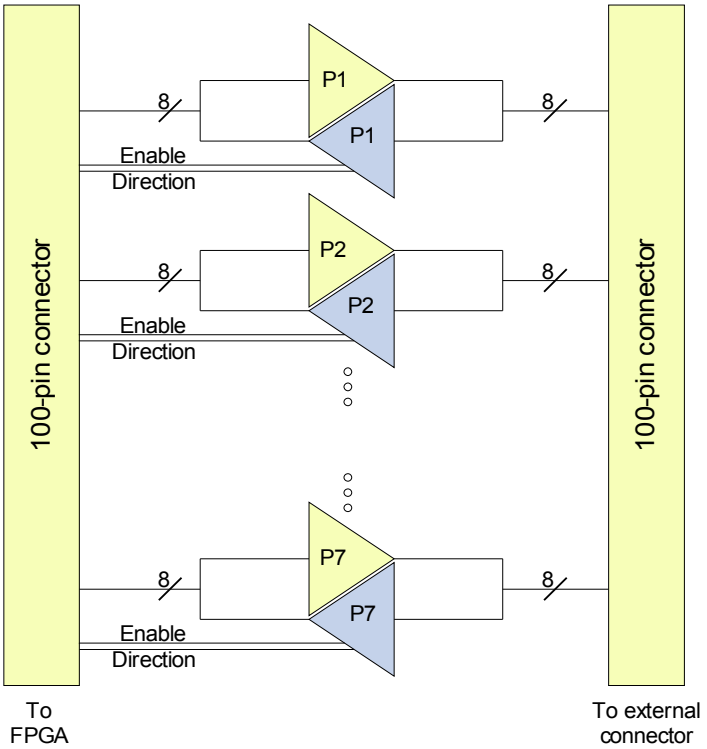
Features

- 8 banks x 8 IOs (5 Volt TTL compatible)
- Each bank configurable as Input or Output
- Individual output-enable for each bank
- Typical output scew per bank < 250 ps
- ESD > 2000V per MIL-STD-883, Method 3015
- ESD >200V using machine model (C=200pF, R=0)
- Balancd output drivers ±24mA
- Uses quadruple of 74FCT162245 Fast CMOS bidirectional transceiver

Requirements

- PCIS3BASE board (CESYS C1010-3105)
- PCIeV4BASE board (CESYS C1080-3807)
  or any other compatible Cesys BASE-board

Block diagram



FPGA balls when used on PCIS3BASE

Pinout PIB64IO on PCIS3BASE					
Signal name	**FPGA IO ball #**	**HD SubD Pin #**	**Signal name**	**FPGA IO ball #**	**HD SubD Pin #**
P0.0	F9	10	P4.0	A11	39
P0.1	L1	9	P4.1	F4	38
P0.2	A8	8	P4.2	B11	37
P0.3	M1	7	P4.3	F3	36
P0.4	B8	6	P4.4	C11	35
P0.5	M2	5	P4.5	F2	34
P0.6	C7	4	P4.6	D11	33
P0.7	M3	3	P4.7	G6	32
DIR P0	E9	--	DIR P4	G5	--
#OE P0	L2	--	#OE P4	E11	--
P1.0	D7	29	P5.0	C12	20
P1.1	M4	28	P5.1	E2	19
P1.2	E7	27	P5.2	D12	18
P1.3	M5	26	P5.3	E1	17
P1.4	F7	25	P5.4	E12	16
P1.5	M6	24	P5.5	F6	15
P1.6	A5	23	P5.6	F12	14
P1.7	N1	22	P5.7	F5	13
DIR P1	N2	--	DIR P5	B12	--
#OE P1	A3	--	#OE P5	E3	--
P2.0	E10	49	P6.0	C13	59
P2.1	K1	48	P6.1	D3	58
P2.2	F10	47	P6.2	D13	57
P2.3	L6	46	P6.3	D2	56
P2.4	A9	45	P6.4	E13	55
P2.5	L5	44	P6.5	D1	54
P2.6	B9	43	P6.6	F13	53
P2.7	L4	42	P6.7	E6	52
DIR P2	L3	--	DIR P6	E4	--
#OE P2	D9	--	#OE P6	A12	--
P3.0	A10	68	P7.0	D14	78
P3.1	H5	67	P7.1	C2	77
P3.2	B10	66	P7.2	E14	76
P3.3	K4	65	P7.3	D6	75
P3.4	C10	64	P7.4	A13	74
P3.5	K3	63	P7.5	D5	73
P3.6	D10	62	P7.6	B13	72
P3.7	K2	61	P7.7	D4	71
DIR P3	F11	--	DIR P7	B14	--
#OE P3	G1	--	#OE P7	C5	--

Pn.x	Signal x of bank n
#OE Pn	active low output enable signal bank n
DIR Pn	bank direction. Low = bank is input (HD-SUB to FPGA) High = bank is output (FPGA to HD-SUB)

FPGA balls when used on PCIeV4BASE

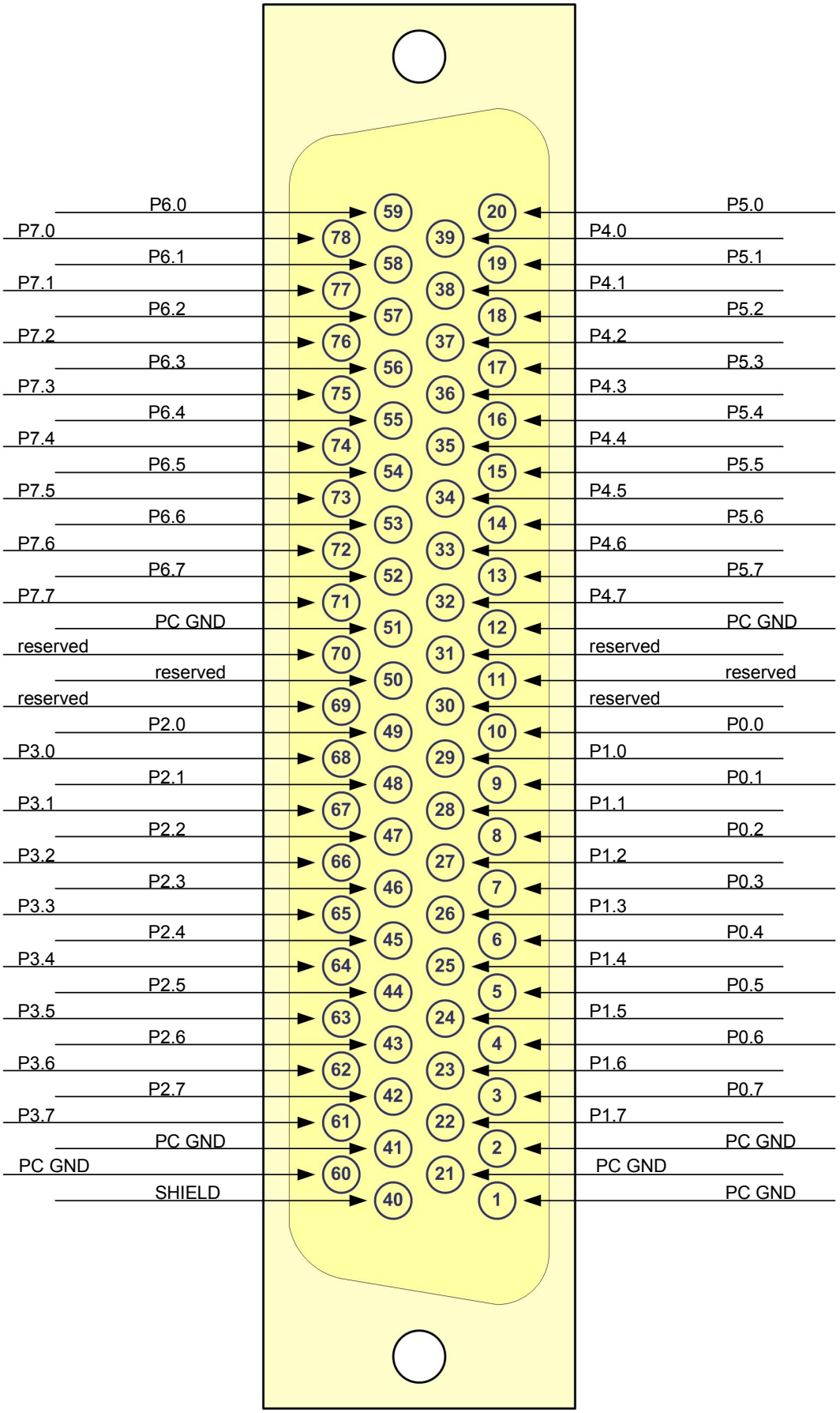
Signal name	FPGA IO ball	HDL Pin	HDL Dir	SubD Pin	Signal name	FPGA IO ball	HDL Pin	HDL Dir	SubD Pin
P0.0	F23	32	I/O	10	P4.0	M19	16	I/O	39
P0.1	H26	58	I/O	9	P4.1	N24	75	I/O	38
P0.2	E23	33	I/O	8	P4.2	K26	17	I/O	37
P0.3	H25	57	I/O	7	P4.3	N23	74	I/O	36
P0.4	E22	34	I/O	6	P4.4	K25	18	I/O	35
P0.5	G26	56	I/O	5	P4.5	N22	73	I/O	34
P0.6	D24	35	I/O	4	P4.6	M23	19	I/O	33
P0.7	G25	55	I/O	3	P4.7	N21	72	I/O	32
DIR P0	F24	31	Out	--	DIR P4	N20	71	Out	--
#OE P0	J22	59	Out	--	#OE P4	M22	20	Out	--
P1.0	C24	36	I/O	29	P5.0	R19	12	I/O	20
P1.1	H24	54	I/O	28	P5.1	P25	79	I/O	19
P1.2	D23	37	I/O	27	P5.2	P19	13	I/O	18
P1.3	H23	53	I/O	26	P5.3	P22	78	I/O	17
P1.4	C23	38	I/O	25	P5.4	P20	14	I/O	16
P1.5	G24	52	I/O	24	P5.5	P23	77	I/O	15
P1.6	A21	39	I/O	23	P5.6	N19	15	I/O	14
P1.7	G23	51	I/O	22	P5.7	N25	76	I/O	13
DIR P1	F26	50	Out	--	DIR P5	R20	11	Out	--
#OE P1	A22	40	Out	--	#OE P5	P24	80	Out	--
P2.0	K20	26	I/O	49	P6.0	R24	6	I/O	59
P2.1	K24	64	I/O	48	P6.1	U23	85	I/O	58
P2.2	K22	27	I/O	47	P6.2	R21	7	I/O	57
P2.3	K23	63	I/O	46	P6.3	T20	84	I/O	56
P2.4	K21	28	I/O	45	P6.4	R22	8	I/O	55
P2.5	J26	62	I/O	44	P6.5	T21	83	I/O	54
P2.6	J21	29	I/O	43	P6.6	T23	9	I/O	53
P2.7	J25	61	I/O	42	P6.7	R25	82	I/O	52
DIR P2	J23	60	Out	--	DIR P6	R26	81	Out	--
#OE P2	J20	30	Out	--	#OE P6	T24	10	Out	--
P3.0	M20	22	I/O	68	P7.0	U22	2	I/O	78
P3.1	M25	68	I/O	67	P7.1	U26	90	I/O	77
P3.2	L21	23	I/O	66	P7.2	T19	3	I/O	76
P3.3	M24	67	I/O	65	P7.3	U24	88	I/O	75
P3.4	L20	23	I/O	64	P7.4	U20	4	I/O	74
P3.5	L24	66	I/O	63	P7.5	U25	87	I/O	73
P3.6	L19	25	I/O	62	P7.6	R23	5	I/O	72
P3.7	L23	65	I/O	61	P7.7	V23	86	I/O	71
DIR P3	M21	21	Out	--	DIR P7	U21	1	Out	--
#OE P3	L26	69	Out	--	#OE P7	V26	91	Out	--

Pn.x	Signal x of bank n
#OE Pn	active low output enable signal bank n
DIR Pn	bank direction. Low = bank is input (HD-SUB to FPGA) High = bank is output (FPGA to HD-SUB)
HDL Pin	Associated I/O number of PIB 93 I/O tri-state bus in demo design
HDL Dir	Static output or dynamic I/O used in demo design

Mounting

Carefully align the mounting holes of the PIB64IO and the BASE board. Firmly press the PIB64IO into its position. Before powering the board make sure, the connectors are aligned correctly and the plug-in-board is not inserted the wrong way.

SUB-D pinout


P6.0
P7.0
P6.1
P7.1
P6.2
P7.2
P6.3
P7.3
P6.4
P7.4
P6.5
P7.5
P6.6
P7.6
P6.7
P7.7
PC GND
reserved
reserved
reserved
P2.0
P3.0
P2.1
P3.1
P2.2
P3.2
P2.3
P3.3
P2.4
P3.4
P2.5
P3.5
P2.6
P3.6
P2.7
P3.7
PC GND
PC GND
SHIELD
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P5.0
P4.0
P5.1
P4.1
P5.2
P4.2
P5.3
P4.3
P5.4
P4.4
P5.5
P4.5
P5.6
P4.6
P5.7
P4.7
PC GND
reserved
reserved
reserved
P0.0
P1.0
P0.1
P1.1
P0.2
P1.2
P0.3
P1.3
P0.4
P1.4
P0.5
P1.5
P0.6
P1.6
P0.7
P1.7
PC GND
PC GND
PC GND

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
10/30/07	1.3	added PCIeV4BASE FPGA ball table updates SUB-D pinout drawing
11/08/07	1.4	fixed PCIeV4BASE FPGA ball table and added HDL IO-Bus information